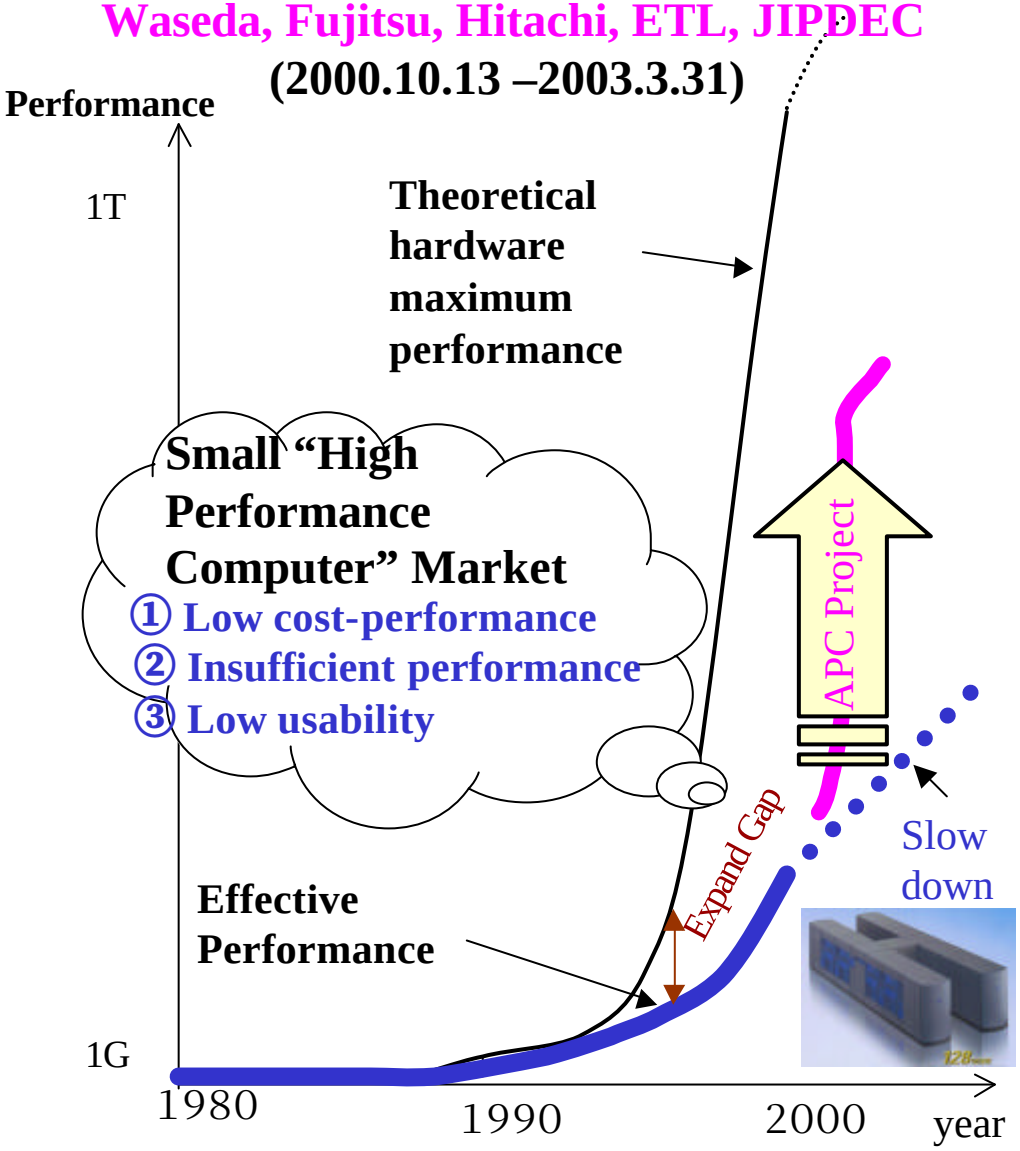
MITI (NEDO) Advanced Parallelizing Compiler Technology Project

Waseda, Fujitsu, Hitachi, ETL, JIPDEC

(2000.10.13 –2003.3.31)



Theoretical maximum performance vs. Effective performance of HPC

Background and Problems

①Adoption of parallel processing as a core technology on PC to HPC

② Increase of importance of software on IT

③ Need for improvement of cost-performance and usability

Contents of Research and Development

① R & D of advanced parallelizing compiler
Multigrain, Data localization, Overhead hiding

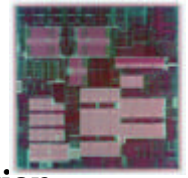
② R & D of Performance evaluation technology for parallelizing compilers

Goal: Double the effective performance

Ripple Effect

① Development of competitive next generation PC and HPC

② Putting the innovative automatic parallelizing compiler technology to practical use



③ Development and market acquisition of future single-chip multiprocessors

④ Boosting R&D in the following many fields:
IT, Bio-tech., Device, Earth environment, Next-generation VLSI design, Financial engineering, Weather forecast, New clean energy, Space development, Automobile, Electric Commerce, etc